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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
ITL.0241D1US

In Re Application Of: **Edward R. Rhoads, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/764,617	January 26, 2004	Zhuo H. Li	21906	2185	8924

Invention: **Organizing Information Stored in Non-Volatile Re-Programmable Semiconductor Memories**

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March 28, 2007

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Dated: **May 8, 2007**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant: Edward R. Rhoads, et al.	§	Art Unit:	2185
Serial No.: 10/764,617	§	Examiner:	Zhuo H. Li
Filed: January 26, 2004	§	Atty Docket:	ITL.0241D1US (P7376D)
For: Organizing Information Stored in Non-Volatile Re-Programmable Semiconductor Memories	§	Assignee:	Intel Corporation

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APPEAL BRIEF

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Nancy Meshkoff

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-15 (Rejected).

Claims 16-25 (Canceled).

Claims 26-30 (Rejected).

Claims 1-15 and 26-30 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments to the claims have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method of organizing stored information on a non-volatile, re-programmable semiconductor memory comprising:

partitioning said memory into a plurality of partitions, each having a defined address (Figure 5, 22) (Specification at page 11, lines 4-25); and

storing the defined address for one partition in another partition (Specification at page 15, lines 1-15).

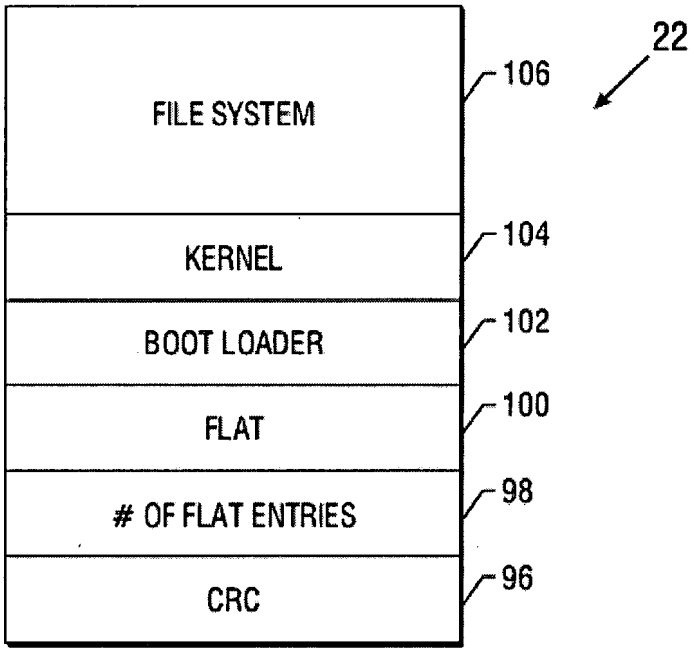

FIG. 5

10. A non-volatile, re-programmable semiconductor memory comprising:

a plurality of addressable partitions (Figure 6, 14), including a partition storing an operating system (Figure 5, 22); and

a storage location storing an address for one of said partitions in association with information about the information stored in said partition (Specification at page 11, lines 4-16, page 12, lines 1-6, and page 15, lines 1-15).

26. A processor-based system comprising:

a processor (Figure 6, 65);

a volatile memory (Figure 6, 68) coupled to said processor; and

a re-programmable, non-volatile semiconductor memory (Figure 5, 96, 98, 100, 102, 104, 106) coupled to said processor, said semiconductor memory including a plurality of partitions (Figure 6, 14), one of said partitions storing an operating system (Figure 5, 22) and another of said partitions (Figure 5, 102) storing the addresses of the other partitions in association with information about what is stored in each of said partitions (Specification at page 11, lines 4-16, page 12, lines 1-6, page 15, lines 1-15).

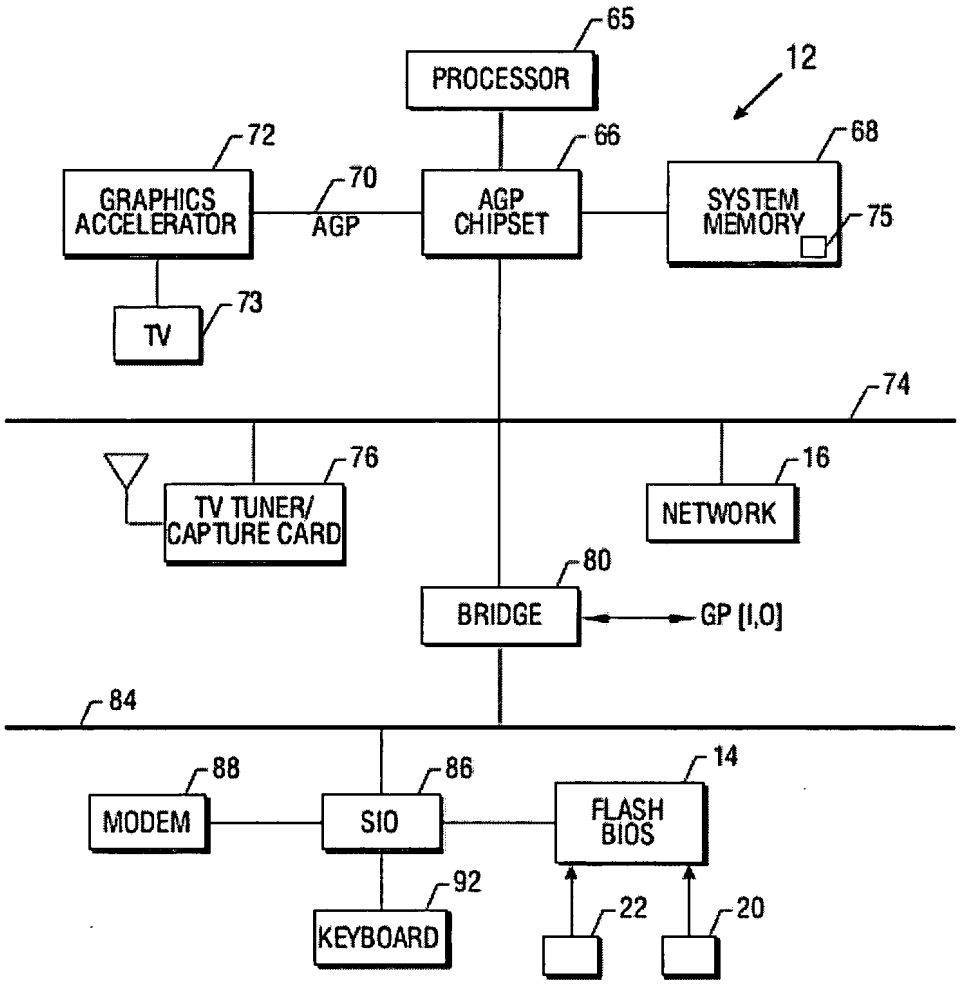

FIG. 6

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Whether claims 1-15 and 26-30 are unpatentable over claims 1-8 of Tallam (US 6,948,099) on the grounds of nonstatutory obviousness-type double patenting.**

B. **Whether claims 1-15 and 26-30 are anticipated under 35 U.S.C. § 102(e) by Tallam (US 6,948,099).**

C. **Whether claims 1-15 and 26-30 are anticipated under 35 U.S.C. § 102(b) by Bunnell (US 5,594,903).**

ARGUMENT

A. Are claims 1-15 and 26-30 unpatentable over claims 1-8 of Tallam (US 6,948,099) on the grounds of nonstatutory obviousness-type double patenting?

Claim 1 of the present application calls for partitioning a memory into a plurality of partitions each having a defined address and storing the defined address for one partition in another partition.

The recited claim of the Tallam patent has nothing to do with storing the defined address for one partition in another partition. For example, the recited claim calls for a first portion of memory storing a recovery operating system and instructions adapted to attain a new operating system "from outside said memory." Thus, this would not constitute defining the defined address for one partition in another partition.

A Declaration under 37 C.F.R. § 1.132 was filed to show that the material in the Tallam application was derived from the inventors Rhoads and Ketrenos in the application drafting process. Namely, a common specification was utilized that combined both separate inventions. However, different claims were provided in the two applications.

A Declaration by one other than the inventor to show attribution is allowed pursuant to M.P.E.P. § 716.10.

The only person who knows what happened here is the undersigned. None of the inventors of either application would have any idea how the application was drafted. Thus, any declaration they could submit would be non-informative.

Moreover, there is no need for any declaration. The M.P.E.P. material relied upon by the Examiner merely states "Moreover, applicant must further show that he or she made the invention upon which the relevant disclosure in the patent, patent publication, or other publication is based [Emphasis added]." There is no reason that this is not fulfilled by the declaration that these inventors filed in the original application claiming that they invented what is claimed or the practitioner's declaration filed with the previous response. In contrast, Tallam also filed a declaration only asserting that he invented what was claimed, which does not include the subject matter claimed in the present application. Thus, there is no inconsistency.

To the extent that a question arises as to how similar material could be in both applications, that has already been explained by the declaration of the prosecuting attorney

submitted previously. Nothing in the cited material and the M.P.E.P. section requires any kind of declaration by anybody. It merely requires the submission of evidence, which evidence has already been submitted by declaration of the prosecuting attorney. The statement that "Moreover, applicant must further show that he or she made the invention upon which the relevant disclosure in the patent application, patent publication, or other publication is based," does not require a declaration of the inventors, but merely a showing by the applicant, which is a broader class. Here, the applicant's attorney has submitted a declaration which explains the situation and the inventors of the present application have filed the only declaration claiming inventorship of the subject matter. That is because the present inventors are the only ones who claim the material and Mr. Tallam did not claim the material at issue.

The assertion that the affidavit submitted by the practitioner is void of facts is untrue. It states that the practitioner used material from the disclosure in this patent application in the preparation of the Tallam application. This explains the inconsistency, but there should really be no issue because there were no claims submitted by Tallam to the subject matter. Therefore, Tallam never filed any declaration saying he invented everything that is in the specification, he only filed a declaration saying he invented what was claimed. Thus, there is no contrary claim to the same subject matter by Tallam.

The assertion that the attorney's allegations that "the authors of the prior art derived the disclosure subject matter" are stated as not being acceptable is confusing since no such statement was ever set forth in the declaration. To the extent this argument was made, it is supported by the declaration that shows that the practitioner used material from the present application in drafting Tallam's application. To the extent that a question is raised as to whether Tallam invented the subject matter in question, the practitioner has explained why the material is in the application and there is no inconsistent claim because Tallam never claimed the material and, therefore, never filed a declaration claiming that he invented it himself. Nothing in any of the material cited in the M.P.E.P. requires inventor declarations.

The assertion that no terminal disclaimer was filed is noted and apparently some confusion arose from the applicant's previous remarks. No terminal disclaimer was filed because it is believed that the double patenting rejection should be reconsidered. For example, in the material in the last office action starting at the bottom of page 9 and bridging over to page 10, it is argued that the double patenting rejection is valid, using arguments based on the disclosure of

Tallam. This is improper. In order to make out a double patenting rejection, the claims must be compared. That was the point made in the previous response. Namely, that "the recited claim of the Tallam patent has nothing to do with storing the defined address for one partition in another partition." For example, the recited claim calls for a first portion of the memory storing a recovery operating system and instructions adapted to attain a new operating system from outside said memory. This would not constitute defining the defined address for one partition in another partition.

In response, the Examiner argues that this is actually found in the specification of Tallam. But that does not matter. In order to support the double patenting rejection, it must be shown that the concept is set forth in the claims, not the disclosure.

B. Are claims 1-15 and 26-30 anticipated under 35 U.S.C. § 102(e) by Tallam (US 6,948,099)?

The Section 102(e) rejection, based on Tallam, is overcome by the attribution or derivation points made above. Namely, that Section 102(e) requires filing by another before the invention by applicant, which did not occur in this case.

C. **Are claims 1-15 and 26-30 anticipated under 35 U.S.C. § 102(b) by Bunnell (US 5,594,903)?**

Finally, turning to the rejection based on Brunnel, it is noted that in the final rejection it is explained that the reliance on Brunnel is based on the language at column 7, lines 50-65 and column 12, lines 42-51.

With respect to the material at column 7, lines 53-65, this is referring to the non-volatile portion 62 which includes the symbols 74 and the data segments 72. But, as clearly shown on the right side of Figure 3, adjacent to the lead line for the element 62, the entire element 62 (including items 72 and 74) is stored in ROM, not RAM. The claim calls for partitioning a non-volatile reprogrammable semiconductor memory. Thus, the material set forth at 62 would not be relevant.

The material cited in column 12 refers to an OS data segment 72' transferred from the non-volatile memory 62, an uninitialized OS ".bss" segment 82, and an image of the operating system symbols 74'. To the extent that the material in the RAM 64 is partitioned, it cannot

possibly include the address for one partition in another partition. If the location 74', for example, includes the address for any other partition, it does not include an address for another partition in the RAM memory, it is simply a copy of the material 74 and then what it best include information about where data segments 72 are in the ROM 62. In other words, it does not store a defined address for one partition in said memory (the non-volatile, reprogrammable memory) in another partition in said memory.

Therefore, the rejection should be reversed.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: May 8, 2007

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CLAIMS APPENDIX

The claims on appeal are:

1. A method of organizing stored information on a non-volatile, re-programmable semiconductor memory comprising:

partitioning said memory into a plurality of partitions, each having a defined address; and

storing the defined address for one partition in another partition.

2. The method of claim 1 further including storing information about the number of partitions.

3. The method of claim 1 further including storing a boot loader in one of said partitions.

4. The method of claim 1 further including storing a file system in one of said partitions.

5. The method of claim 1 further including storing a kernel for an operating system in one of said partitions.

6. The method of claim 1 further including storing information in association with said addresses about whether or not an integrity check needs to be done on the data stored at the associated address.

7. The method of claim 1 further including storing, in association with the address of a partition, information about the type of information stored in the partition.

8. The method of claim 7 further including storing information about whether or not the information stored at a given partition is a boot loader, a kernel or a file system.

9. The method of claim 7 including storing information about the load address for said information in association with said address.

10. A non-volatile, re-programmable semiconductor memory comprising:

a plurality of addressable partitions, including a partition storing an operating system; and

a storage location storing an address for one of said partitions in association with information about the information stored in said partition.

11. The memory of claim 10 wherein said memory is a FLASH memory.

12. The memory of claim 10 wherein one of said partitions stores a basic input/output system.

13. The memory of claim 10 wherein one of said partitions stores a file system.

14. The memory of claim 10 wherein one of said partitions stores a kernel for an operating system.

15. The memory of claim 10 wherein one of said partitions stores a boot loader.

26. A processor-based system comprising:

a processor;

a volatile memory coupled to said processor; and

a re-programmable, non-volatile semiconductor memory coupled to said processor, said semiconductor memory including a plurality of partitions, one of said partitions storing an operating system and another of said partitions storing the addresses of the other partitions in association with information about what is stored in each of said partitions.

27. The system of claim 26 wherein said semiconductor memory is a FLASH memory.

28. The system of claim 26 wherein one of said partitions stores a basic input/output system.

29. The system of claim 26 wherein one of said partitions stores a file system.

30. The system of claim 26 wherein one of said partitions stores a boot loader.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.